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10/051,222	01/18/2002	Jinghui Lu	X-1055 US	7174

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,222	LU ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-15-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The oath or declaration of records is unsigned. The Examiner contact the Applicant's representative on 06/21/05 and he agreed to resend the Applicant Response to Pre-Exam Formalities Notice sent on 04/23/2002 by fax.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "108" has been used to designate both correction block of 102 and correction block of 106. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 110 (see specification paragraphs [0044] and [0045]. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: in line 6 of paragraph [0064l the recitation "programmable gain network 154" is improper; it is suggested to be changed to "programmable gain network 254" (see figure 12).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 8-10, 15, 16, 21-25, 27 and 30-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimamoto (US 6147672).

As per claim 1 Shimamoto discloses an integrated high-speed parallel-to-serial and serial-to-parallel transceiver, wherein the transceiver comprises a receiver section that includes a receiver clocking circuit operably coupled to produce at least one high frequency receiver clock (figure 3 column 3 lines 1-56 and column 6 lines 15-67); serial

to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency receiver clock (figure 3 block 20 column 3 lines 1-56 and column 6 lines 15-67); and receiver compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at least one of the receiver clocking circuit and the serial to parallel module (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); transmitter section that includes: transmitter clocking circuit operably coupled to produce at least one high frequency transmitter clock (figure 2 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency transmitter clock (figure 2 block 7 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); and transmitter compensation operable to at least partially compensate for at least one of the integrated circuit operational limitations and the integrated circuit fabrication limitations of at least one of the transmitter clocking circuit and the parallel to serial module (figure 2 blocks 9-12 column 3 lines 1-56 and column 5 line 40 to column 6 line 14).

As per claim 2 Shimamoto discloses claim 1. Shimamoto also discloses that serial to parallel module and the receiver compensation further comprise an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data (figures 3 and 6 block 15 column 3 lines 1-56

and column 6 lines 15-67 and column 7 lines 27-37); even serial to parallel converter operably coupled to convert the serial even data into parallel even data (figures 3 and 6 block 20 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data (figures 3 and 6 block 19 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); and output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data (figures 3 and 6 block 17 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37).

As per claim 4 Shimamoto discloses claim 2. Shimamoto also discloses the use of a plurality of interoperably coupled high-speed, low power, differential flip flops (figure 7 column 7 line 27 to column 8 line 47).

As per claim 8 Shimamoto discloses claim 1. Shimamoto also discloses an interface operably coupled to receive the outbound parallel data (figures 5 and 7 block 1 column 7 line 27 to column 8 line 57); even parallel to serial converter operably coupled to convert an even portion of the outbound parallel data into even serial outbound data (figures 5 and 7 block 6 column 7 line 27 to column 8 line 57); odd parallel to serial converter operably coupled to convert an odd portion of the outbound parallel data into odd serial outbound data (figures 5 and 7 block 5 column 7 line 27 to column 8 line 57); combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data (figures 5 and 7 block 3 column 7 line 27 to column 8 line 57); and driver operably coupled to produce the outbound serial data from

the combined serial data (figures 5 and 7 blocks 61, 33, 35, 41 column 7 line 27 to column 8 line 57).

As per claim 9 Shimamoto discloses claim 8. Shimamoto also discloses differential input interface having a calibrated input impedance (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57); and buffer operably coupled to temporarily store the outbound parallel data received via the differential input interface (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 10 Shimamoto discloses claim 8. Shimamoto also discloses each of the even and add parallel to serial converters further comprises a plurality of interoperably coupled high-speed, low power, differential flip flops (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 15 Shimamoto discloses a high-speed parallel-to-serial and serial-to-parallel transceiver, where the transceiver comprises clocking circuit operably coupled to produce at least one high frequency clock (figure 2 block 8 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency clock (figure 3 block 20 column 3 lines 1-56 and column 6 lines 15-67); parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency clock (figure 2 block 7 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); and compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at

least one of the clocking circuit, the parallel to serial module, and the serial to parallel module (figure 2 blocks 9-12 column 3 lines 1-56 and column 5 line 40 to column 6 line 14 figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67).

As per claim 16 Shimamoto discloses claim 15. Shimamoto also discloses an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data (figures 3 and 6 block 15 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); even serial to parallel converter operably coupled to convert the serial even data into parallel even data (figures 3 and 6 block 20 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data (figures 3 and 6 block 19 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); and output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data (figures 3 and 6 block 17 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37).

As per claim 21 Shimamoto discloses claim 15. Shimamoto also discloses an interface operably coupled to receive the outbound parallel data (figures 5 and 7 block 1 column 7 line 27 to column 8 line 57); even parallel to serial converter operably coupled to convert an even portion of the outbound parallel data into even serial outbound data (figures 5 and 7 block 6 column 7 line 27 to column 8 line 57); odd parallel to serial converter operably coupled to convert an odd portion of the outbound parallel data into

odd serial outbound data (figures 5 and 7 block 5 column 7 line 27 to column 8 line 57); combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data (figures 5 and 7 block 3 column 7 line 27 to column 8 line 57); and driver operably coupled to produce the outbound serial data from the combined serial data (figures 5 and 7 blocks 61, 33, 35, 41 column 7 line 27 to column 8 line 57).

As per claim 22 Shimamoto discloses claim 21. Shimamoto also discloses differential input interface having a calibrated input impedance (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57); and buffer operably coupled to temporarily store the outbound parallel data received via the differential input interface (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 23 Shimamoto discloses claim 22. Shimamoto also discloses each of the even and add parallel to serial converters further comprises a plurality of interoperably coupled high-speed, low power, differential flip flops (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 24 Shimamoto discloses an integrated high-speed wherein the receiver comprises clocking circuit operably coupled to produce at least one high frequency clock (figure 3 block 21 column 3 lines 1-56 and column 6 lines 15-67); serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency clock (figure 3 block 20 column 3 lines 1-56 and column 6 lines 15-67); and compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and

integrated circuit fabrication limitations of at least one of the clocking circuit and the serial to parallel module. serial-to-parallel receiver(figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67).

As per claim 25 Shimamoto discloses claim 24. Shimamoto also discloses that serial to parallel module and the receiver compensation further comprise an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data (figures 3 and 6 block 15 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); even serial to parallel converter operably coupled to convert the serial even data into parallel even data (figures 3 and 6 block 20 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data (figures 3 and 6 block 19 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); and output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data (figures 3 and 6 block 17 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37).

As per claim 27 Shimamoto discloses claim 25. Shimamoto also discloses the use of a plurality of interoperably coupled high-speed, low power, differential flip flops (figure 7 column 7 line 27 to column 8 line 47).

As per claim 30 Shimamoto discloses an integrated high-speed parallel-to-serial transmitter, where the transmitter comprises clocking circuit operably coupled to

produce at least one high frequency clock (figure 2 block 8 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency clock (figure 2 block 7 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); and compensation operable to least partially compensate for at least one of the integrated circuit operational limitations and the integrated circuit fabrication limitations of at least one of the clocking circuit and the parallel to serial module (figure 2 blocks 9-12 column 3 lines 1-56 and column 5 line 40 to column 6 line 14).

As per claim 31 Shimamoto discloses claim 30. Shimamoto also discloses an interface operably coupled to receive the outbound parallel data (figures 5 and 7 block 1 column 7 line 27 to column 8 line 57); even parallel to serial converter operably coupled to convert an even portion of the outbound parallel data into even serial outbound data (figures 5 and 7 block 6 column 7 line 27 to column 8 line 57); odd parallel to serial converter operably coupled to convert an odd portion of the outbound parallel data into odd serial outbound data (figures 5 and 7 block 5 column 7 line 27 to column 8 line 57); combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data (figures 5 and 7 block 3 column 7 line 27 to column 8 line 57); and driver operably coupled to produce the outbound serial data from the combined serial data (figures 5 and 7 blocks 61, 33, 35, 41 column 7 line 27 to column 8 line 57).

As per claim 32 Shimamoto discloses claim 31. Shimamoto also discloses differential input interface having a calibrated input impedance (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57); and buffer operably coupled to temporarily store the outbound parallel data received via the differential input interface (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 33 Shimamoto discloses claim 31. Shimamoto also discloses each of the even and add parallel to serial converters further comprises a plurality of interoperably coupled high-speed, low power, differential flip flops (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 17, 18 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) as applied to claim 2 above, and further in view of Ipek (US 20010018334).

As per claim 3 Shimamoto discloses claim 2. Shimamoto also discloses an interface and an amplifier (figure 3 blocks 15 and 22-26 column 3 lines 1-56 and column 5 line 40 to column 6 line 14). Shimamoto doesn't disclose an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier. Ipek discloses an inductive amplifier operably coupled to the

interface and a feed forward boost module operably coupled to the inductive amplifier (figure 1 paragraphs [0013] to [0025]). Shimamoto and Ipek are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto boosted inductive amplifier disclosed by Ipek. The suggestion/motivation for doing so would have been to design a receiver with a large dynamic range and a high linearity, and having a low noise (Ipek abstract). Therefore, it would have been obvious to combine Shimamoto with Ipek to obtain the invention as specified in claim 3.

As per claim 17 Shimamoto discloses claim 16. Shimamoto also discloses an interface and an amplifier (figure 3 blocks 15 and 22-26 column 3 lines 1-56 and column 5 line 40 to column 6 line 14). Shimamoto doesn't disclose an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier. Ipek discloses an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier (figure 1 paragraphs [0013] to [0025]). Shimamoto and Ipek are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto boosted inductive amplifier disclosed by Ipek. The suggestion/motivation for doing so would have been to design a receiver with a large dynamic range and a high linearity, and having a low noise (Ipek abstract). Therefore, it

would have been obvious to combine Shimamoto with Ipek to obtain the invention as specified in claim 17.

As per claim 18 Shimamoto and Ipek disclose claim 17. Shimamoto also discloses the use of a plurality of interoperably coupled high-speed, low power, differential flip flops (figure 7 column 7 line 27 to column 8 line 47). Shimamoto and Ipek are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto boosted inductive amplifier disclosed by Ipek. The suggestion/motivation for doing so would have been to design a receiver with a large dynamic range and a high linearity, and having a low noise (Ipek abstract). Therefore, it would have been obvious to combine Shimamoto with Ipek to obtain the invention as specified in claim 18.

As per claim 26 Shimamoto discloses claim 25. Shimamoto also discloses an interface and an amplifier (figure 3 blocks 15 and 22-26 column 3 lines 1-56 and column 5 line 40 to column 6 line 14). Shimamoto doesn't disclose an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier. Ipek discloses an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier (figure 1 paragraphs [0013] to [0025]). Shimamoto and Ipek are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto boosted inductive amplifier disclosed by Ipek. The

suggestion/motivation for doing so would have been to design a receiver with a large dynamic range and a high linearity, and having a low noise (Ipek abstract). Therefore, it would have been obvious to combine Shimamoto with Ipek to obtain the invention as specified in claim 26.

Claims 5, 7, 11, 19, 28 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) as applied to claim 1 above, and further in view of Welland (US 6167245).

As per claim 5 Shimamoto discloses claim 1. Shimamoto doesn't disclose a fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock; fine charge pump operably coupled to produce a voltage representative of the fine difference signal; coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock; coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal; filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal produce a filtered difference representation; voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation; post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock; coarse divider operably coupled to produce the coarse feedback clock

from the at least one high frequency receiver clock.. Welland discloses a fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock (figure 1-6 block 402 column 5 line 54 to column 12 line 18); fine charge pump operably coupled to produce a voltage representative of the fine difference signal (figure 1-6 block 402 column 5 line 54 to column 12 line 18); coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18); coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal (figure 1-6 block 406 column 5 line 54 to column 12 line 18); filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal produce a filtered difference representation (figure 1-6 block 210 column 5 line 54 to column 12 line 18); voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation (figure 1-6 block 400 column 5 line 54 to column 12 line 18); post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock (figure 1-6 block 624 column 5 line 54 to column 12 line 18); coarse divider operably coupled to produce the coarse feedback clock from the at least one high frequency receiver clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are from

the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 5.

As per claim 7 Shimamoto and Welland discloses claim 5. Welland also discloses critical analog high frequency receiver clock (figure 1-6 block 106 column 5 line 54 to column 12 line 18); analog high frequency receiver clock (figure 1-6 block 400 column 5 line 54 to column 12 line 18); and digital high frequency receiver clock (figure 1-6 block 400 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 7.

As per claim 11 Shimamoto discloses claim 1. Shimamoto doesn't disclose a phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference lock and a feedback clock that is representative of the

at Least one high frequency transmitter clock; charge pump operably coupled to produce a voltage representative of the difference signal; filter operably coupled filter the voltage representation of the difference signal to produce a filtered difference representation; voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation; post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock; and divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock. Welland discloses phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference lock and a feedback clock that is representative of the at Least one high frequency transmitter clock (figure 1-6 block 402 column 5 line 54 to column 12 line 18); charge pump operably coupled to produce a voltage representative of the difference signal (figure 1-6 block 402 column 5 line 54 to column 12 line 18); filter operably coupled filter the voltage representation of the difference signal to produce a filtered difference representation (figure 1-6 block 210 column 5 line 54 to column 12 line 18); voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation (figure 1-6 block 400 column 5 line 54 to column 12 line 18); post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock (figure 1-6 block 624 column 5 line 54 to column 12 line 18); and divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are

from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 11.

As per claim 19 Shimamoto discloses claim 15. Shimamoto doesn't disclose a fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock; fine charge pump operably coupled to produce a voltage representative of the fine difference signal; coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock; coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal; filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal produce a filtered difference representation; voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation; post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock; coarse divider operably coupled to produce the coarse feedback clock

from the at least one high frequency receiver clock.. Welland discloses a fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock (figure 1-6 block 402 column 5 line 54 to column 12 line 18); fine charge pump operably coupled to produce a voltage representative of the fine difference signal (figure 1-6 block 402 column 5 line 54 to column 12 line 18); coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18); coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal (figure 1-6 block 406 column 5 line 54 to column 12 line 18); filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal produce a filtered difference representation (figure 1-6 block 210 column 5 line 54 to column 12 line 18); voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation (figure 1-6 block 400 column 5 line 54 to column 12 line 18); post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock (figure 1-6 block 624 column 5 line 54 to column 12 line 18); coarse divider operably coupled to produce the coarse feedback clock from the at least one high frequency receiver clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are from

the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 19.

As per claim 28 Shimamoto discloses claim 24. Shimamoto doesn't disclose a fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock; fine charge pump operably coupled to produce a voltage representative of the fine difference signal; coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock; coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal; filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal produce a filtered difference representation; voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation; post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock; coarse divider operably coupled to produce the coarse feedback clock

from the at least one high frequency receiver clock.. Welland discloses a fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock (figure 1-6 block 402 column 5 line 54 to column 12 line 18); fine charge pump operably coupled to produce a voltage representative of the fine difference signal (figure 1-6 block 402 column 5 line 54 to column 12 line 18); coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18); coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal (figure 1-6 block 406 column 5 line 54 to column 12 line 18); filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal produce a filtered difference representation (figure 1-6 block 210 column 5 line 54 to column 12 line 18); voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation (figure 1-6 block 400 column 5 line 54 to column 12 line 18); post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock (figure 1-6 block 624 column 5 line 54 to column 12 line 18); coarse divider operably coupled to produce the coarse feedback clock from the at least one high frequency receiver clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are from

the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 28.

As per claim 34 Shimamoto discloses claim 30. Shimamoto doesn't disclose a phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference lock and a feedback clock that is representative of the at Least one high frequency transmitter clock; charge pump operably coupled to produce a voltage representative of the difference signal; filter operably coupled filter the voltage representation of the difference signal to produce a filtered difference representation; voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation; post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock; and divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock. Welland discloses phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference lock and a feedback clock that is representative of the at Least one high frequency transmitter clock (figure 1-6 block 402 column 5 line 54 to column 12 line 18); charge pump operably coupled to produce a voltage representative of the difference

signal (figure 1-6 block 402 column 5 line 54 to column 12 line 18); filter operably coupled filter the voltage representation of the difference signal to produce a filtered difference representation (figure 1-6 block 210 column 5 line 54 to column 12 line 18); voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation (figure 1-6 block 400 column 5 line 54 to column 12 line 18); post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock (figure 1-6 block 624 column 5 line 54 to column 12 line 18); and divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 34.

Claims 6, 13, 14, 20 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) in view of Welland (US 6167245) as applied to claim 5 above, and further in view of Kim (US 20010030562).

As per claim 6 Shimamoto and Welland discloses claim 5. Shimamoto and Welland don't disclose a duty cycle distortion correction module operably coupled to

compensate for duty cycle distortion of a differential representation of the at least one high frequency clock. Kim discloses a duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock (figure 8 paragraphs [0043] to [0046]. Shimamoto, Welland and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 6.

As per claim 13 Shimamoto and Welland discloses claim 11. Shimamoto and Welland don't disclose a duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock. Kim discloses a duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock (figure 8 paragraphs [0043] to [0046]. Shimamoto, Welland and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would

have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 13.

As per claim 14 Shimamoto, Welland and Kim discloses claim 13. Welland also discloses a phase error correction circuit operably coupled to correct phase error of the at least one high frequency transmitter clock (figure 1-6 block 206 column 5 line 54 to column 12 line 18). Shimamoto, Welland and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 14.

As per claim 20 Shimamoto and Welland discloses claim 19. Shimamoto and Welland don't disclose a duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock. Kim discloses a duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock (figure 8 paragraphs [0043] to [0046]. Shimamoto, Welland and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for

doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 20.

As per claim 29 Shimamoto and Welland discloses claim 28. Shimamoto and Welland don't disclose a duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock. Kim discloses a duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock (figure 8 paragraphs [0043] to [0046]. Shimamoto, Welland and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 29.

Claims 12 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) in view of Welland (US 6167245) as applied to claim 11 above, and further in view of Mohindra (US 6148047).

As per claim 12 Shimamoto and Welland disclose claim 11. Shimamoto and Welland don't disclose an offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation. Mohindra discloses

offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation (figure 8 column 6 lines 8-61). Shimamoto, Welland and Mohindra are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the DC offset compensation disclosed by Mohindra. The suggestion/motivation for doing so would have been to reduce distortion of the signal (Mohindra column 1 lines 36-42). Therefore, it would have been obvious to combine Shimamoto and Welland with Mohindra to obtain the invention as specified in claim 12.

As per claim 35 Shimamoto and Welland disclose claim 34. Shimamoto and Welland don't disclose an offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation. Mohindra discloses offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation (figure 8 column 6 lines 8-61). Shimamoto, Welland and Mohindra are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the DC offset compensation disclosed by Mohindra. The suggestion/motivation for doing so would have been to reduce distortion of the signal (Mohindra column 1 lines 36-42). Therefore, it would have been obvious to combine Shimamoto and Welland with Mohindra to obtain the invention as specified in claim 35.

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) in view of Welland (US 6167245) and Mohindra (US 6148047) as applied to claim 35 above, and further in view of Kim (US 20010030562).

As per claim 36 Shimamoto, Welland and Mohindra disclose claim 35. Shimamoto, Welland and Mohindra don't disclose a duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock. Kim discloses a duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock (figure 8 paragraphs [0043] to [0046]. Shimamoto, Welland, Mohindra and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto, Welland and Mohindra with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto, Welland and Mohindra with Kim to obtain the invention as specified in claim 36.

As per claim 37 Shimamoto, Welland, Mohindra and Kim discloses claim 36. Welland also discloses a phase error correction circuit operably coupled to correct phase error of the at least one high frequency transmitter clock (figure 1-6 block 206 column 5 line 54 to column 12 line 18). Shimamoto, Welland, Mohindra and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine

in the transceiver circuit disclosed by Shimamoto, Welland and Mohindra with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 37.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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06-21-2005

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